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NGO, NGUYEN HOANG	
ART UNIT	**PAPER NUMBER**
2663	

DATE MAILED: 12/13/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/998,523	SHARMA ET AL.	
	Examiner	Art Unit	
	Nguyen Ngo	2663	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *28 September 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-14* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *8-11* is/are allowed.

6)☒ Claim(s) *1-7 and 12-14* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

1. This communication is in response to the amendment of 9/28/2005. All changes made to the claims have been entered. Accordingly, Claims 1-14 are currently pending in the application.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

4. Claims 1-7 and 12-14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Cisneros (US 5157654) in view of Iyer, Sundar et al. (Analysis of a packet switch with memories running slower than the line-rate; Computer Systems Laboratory, Stanford University), hereinafter referred to as Cisneros and Iyer.

Regarding claim 1, Cisneros discloses an apparatus comprising:

planes of self-routing cross-points switching planes (cross bar switches, 550 of figure 5) with each plane having separate input and separate output connections (each cross bar switch having a plurality of switch input ports and a plurality of switch output ports, col17 lines 57-60). It is further seen from figure 5 that each switch input port (I1 to Ik) is coupled to and associated with a plurality of input data queues (queues in input module).

input modules, wherein each input modules contains a single queue, that successively reads the current incoming ATM cells appearing at each of its inputs and deposits the cell into the next available location in the queue (col20 lines 9-16), wherein the input modules feeds the input of each of the different switching planes (a plurality of input data queues, each input data queue having an input port capable of receiving data packets, each of said input data queues also having an output port coupled to a corresponding switch input port (O1 to Om (output port) of a specific queue coupled to different cross-point planes through I1 to Ik (input port)) of a corresponding cross bar switch, 260 of figure 5 and col19 lines3-6).

demultiplexers which accepts incoming cells from user lines and demultiplexes the cells occurring at the STS-48 rate and appearing on single incoming lines, on a 1-to-16 basis, into separate bit-serial lines feeding the input modules (a plurality of data demultiplexers, each data demultiplexer having a data input port at which a data stream S (single incoming line) is received, and each demulitplexer having a plurality of data output ports, as seen from 230 of figure 2 and col13 lines48-55).

a control switch module coupled to the switch fabric containing input modules and coupled to the demultiplexers (figure 2) which controls each of the blocks that constitute the switch, for example, processes incoming calls by establishing and tearing down appropriate virtual connections through the switch (global scheduler operatively coupled to said data demultiplexers and to each of said data input data queues, controlling the routing of data from said plurality of switch input ports to said plurality of switch output ports, col12 lines56-68).

Cisneros however fails to specifically disclose each demultiplexer having a plurality of data output ports each of which is coupled to a separate one of the input data queues associated with each corresponding cross bar switch input port. Cisneros however discloses of deficiencies of switches can be ameliorated through various queuing functions and centralized control (col4 lines 34-39), thus providing the motivation to improve speeds of a switching system in a efficient and reliable manner.

Iyer further discloses the desire to build a very high speed packet-switch with extremely high line-rates, by building a packet-switch from multiple, lower speed packet-switches in parallel (abstract). From figure 1, discloses of a parallel packet switch architecture that when a cell arrives at an input port, the demulitplexer selects a layer (cross point plane) to send the cell to and that each of the layers receive cells from the N input ports, then switches each cell to its output port (page 3). It should be seen from figure 1 and figure 2, of an architecture that discloses each demultiplexer having a

plurality of data output ports each of which is coupled to a separate one of the input data queues associated with each corresponding cross bar switch input port. It would thus be obvious to a person skilled in the art to incorporate the architecture of a switching system as disclosed by Iyer into the apparatus and method for a large packet switch which utilizes cell address look-ahead in conjunction with parallel cross point planes as disclosed by Cisneros to efficiently improve the speed of a packet system in a reliable manner, more specifically the coupling of demultiplexer output ports to different switching layers and the switching plane's associated queue.

Regarding claim 2, Cisneros discloses an apparatus comprising;

planes of self-routing cross-points switching planes (cross bar switches, 550 of figure 5) with each plane having separate input and separate output connections (each cross bar switch having a plurality of switch input ports and a plurality of switch output ports, col17 lines 57-60). It is further seen from figure 5 that each switch input port (I1 to Ik) is coupled to and associated with a plurality of input data queues (queues in input module).

input modules, wherein each input modules contains a single queue, that successively reads the current incoming ATM cells appearing at each of its inputs and deposits the cell into the next available location in the queue (col20 lines 9-16), wherein the input modules feeds the input of each of the different switching planes (a plurality of input data queues, each input data queue having an input port capable of receiving data

packets, each of said input data queues also having an output port coupled to a corresponding switch input port (O1 to Om (output port) of a specific queue coupled to different cross-point planes through I1 to Ik (input port)) of a corresponding cross bar switch, 260 of figure 5 and col19 lines3-6).

demultiplexers which accepts incoming cells from user lines and demultiplexes the cells occurring at the STS-48 rate and appearing on single incoming lines, on a 1-to-16 basis, into separate bit-serial lines feeding the input modules (a plurality of data demultiplexers, each data demultiplexer having a data input port at which a data stream S (single incoming line) is received, and each demulitplexer having a plurality of data output ports, as seen from 230 of figure 2 and col13 lines48-55).

a control switch module coupled to the switch fabric containing input modules and coupled to the demultiplexers (figure 2) which controls each of the blocks that constitute the switch, for example, processes incoming calls by establishing and tearing down appropriate virtual connections through the switch (global scheduler operatively coupled to said data demultiplexers and to each of said data input data queues, controlling the routing of data from said plurality of switch input ports to said plurality of switch output ports, col12 lines56-68).

a header processing unit formed of input buffer which provides sufficient time to perform table look up operations to translate the current VCI for an incoming cell and formulate an appropriate routing header for that cell in conjunction with the switch control module (col15 lines 35-56) and that the routing header is strictly for internal use in routing the entire cell through the switch (examining cells (header processing) at the

heads of the data demultiplexer and determine from data in said cells, which switch input port of a cross bar switch should be coupled to a particular switch output port of the crossbar switch (routing), col11 lines50-59). It is noted that the examining of the cells may be done at any component of the switching system as this is well known in the art.

Cisneros however fails to specifically disclose each demultiplexer having a plurality of data output ports each of which is coupled to a separate one of the input data queues associated with each corresponding cross bar switch input port. Cisneros however discloses of deficiencies of switches can be ameliorated through various queuing functions and centralized control (col4 lines 34-39), thus providing the motivation to improve speeds of a switching system in a efficient and reliable manner.

Iyer further discloses the desire to build a very high speed packet-switch with extremely high line-rates, by building a packet-switch from multiple, lower speed packet-switches in parallel (abstract). From figure 1, discloses of a parallel packet switch architecture that when a cell arrives at an input port, the demulitplexer selects a layer (cross point plane) to send the cell to and that each of the layers receive cells from the N input ports, then switches each cell to its output port (page 3). It should be seen from figure 1 and figure 2, of an architecture that discloses each demultiplexer having a plurality of data output ports each of which is coupled to a separate one of the input data queues associated with each corresponding cross bar switch input port. It would thus be obvious to a person skilled in the art to incorporate the architecture of a

switching system as disclosed by Iyer into the apparatus and method for a large packet switch which utilizes cell address look-ahead in conjunction with parallel cross point planes as disclosed by Cisneros to efficiently improve the speed of a packet system in a reliable manner, more specifically the coupling of demultiplexer output ports to different switching layers and the switching plane's associated queue

Regarding claim 3, Cisneros discloses an apparatus comprising:

planes of self-routing cross-points switching planes (cross bar switches, 550 of figure 5) with each plane having separate input and separate output connections (each cross bar switch having a plurality of switch input ports and a plurality of switch output ports, col17 lines 57-60). It is further seen from figure 5 that each switch input port (I1 to Ik) is coupled to and associated with a plurality of input data queues (queues in input module).

input modules, wherein each input modules contains a single queue, that successively reads the current incoming ATM cells appearing at each of its inputs and deposits the cell into the next available location in the queue (col20 lines 9-16), wherein the input modules feeds the input of each of the different switching planes (a plurality of input data queues, each input data queue having an input port capable of receiving data packets, each of said input data queues also having an output port coupled to a corresponding switch input port (O1 to Om (output port) of a specific queue coupled to different cross-point planes through I1 to Ik (input port)) of a corresponding cross bar switch, 260 of figure 5 and col19 lines3-6).

demultiplexers which accepts incoming cells from user lines and demultiplexes the cells occurring at the STS-48 rate and appearing on single incoming lines, on a 1-to-16 basis, into separate bit-serial lines feeding the input modules (a plurality of data demultiplexers, each data demultiplexer having a data input port at which a data stream S (single incoming line) is received, and each demulitplexer having a plurality of data output ports, as seen from 230 of figure 2 and col13 lines48-55).

a control switch module coupled to the switch fabric containing input modules and coupled to the demultiplexers (figure 2) which controls each of the blocks that constitute the switch, for example, processes incoming calls by establishing and tearing down appropriate virtual connections through the switch (global scheduler operatively coupled to said data demultiplexers and to each of said data input data queues, controlling the routing of data from said plurality of switch input ports to said plurality of switch output ports, col12 lines56-68).

a header processing unit formed of input buffer which provides sufficient time to perform table look up operations to translate the current VCI for an incoming cell and formulate an appropriate routing header for that cell in conjunction with the switch control module (col15 lines 35-56) and that the routing header is strictly for internal use in routing the entire cell through the switch (examining cells (header processing) at the heads of the data demultiplexer and determine from data in said cells, which switch input port of a cross bar switch should be coupled to a particular switch output port of the crossbar switch (routing), col11 lines50-59). It is noted that the examining of the

cells may be done at any component of the switching system as this is well known in the art.

that the header processing unit is connected to the switch control module for receiving control instructions which controls the demultiplexing of the cell traffic on the line across separate lines (col15 line 11-14), and the header processing unit translates the current VCI with the new VCI and prepends an appropriate routing header onto the cell for routing (configure said data demultiplexers so as to route data cells of a particular incoming data flow to an appropriate input data queue, col15 lines 29-32).

Cisneros however fails to specifically disclose each demultiplexer having a plurality of data output ports each of which is coupled to a separate one of the input data queues associated with each corresponding cross bar switch input port. Cisneros however discloses of deficiencies of switches can be ameliorated through various queuing functions and centralized control (col4 lines 34-39), thus providing the motivation to improve speeds of a switching system in a efficient and reliable manner.

Iyer further discloses the desire to build a very high speed packet-switch with extremely high line-rates, by building a packet-switch from multiple, lower speed packet-switches in parallel (abstract). From figure 1, discloses of a parallel packet switch architecture that when a cell arrives at an input port, the demulitplexer selects a layer (cross point plane) to send the cell to and that each of the layers receive cells from the N input ports, then switches each cell to its output port (page 3). It should be seen from

figure 1 and figure 2, of an architecture that discloses each demultiplexer having a plurality of data output ports each of which is coupled to a separate one of the input data queues associated with each corresponding cross bar switch input port. It would thus be obvious to a person skilled in the art to incorporate the architecture of a switching system as disclosed by Iyer into the apparatus and method for a large packet switch which utilizes cell address look-ahead in conjunction with parallel cross point planes as disclosed by Cisneros to efficiently improve the speed of a packet system in a reliable manner, more specifically the coupling of demultiplexer output ports to different switching layers and the switching plane's associated queue

Regarding claim 4, Cisneros discloses an apparatus comprising:

planes of self-routing cross-points switching planes (cross bar switches, 550 of figure 5) with each plane having separate input and separate output connections (each cross bar switch having a plurality of switch input ports and a plurality of switch output ports, col17 lines 57-60). It is further seen from figure 5 that each switch input port (I1 to Ik) is coupled to and associated with a plurality of input data queues (queues in input module).

input modules, wherein each input modules contains a single queue, that successively reads the current incoming ATM cells appearing at each of its inputs and deposits the cell into the next available location in the queue (col20 lines 9-16), wherein the input modules feeds the input of each of the different switching planes (a plurality of

input data queues, each input data queue having an input port capable of receiving data packets, each of said input data queues also having an output port coupled to a corresponding switch input port (O1 to Om (output port) of a specific queue coupled to different cross-point planes through I1 to Ik (input port)) of a corresponding cross bar switch, 260 of figure 5 and col19 lines3-6).

demultiplexers which accepts incoming cells from user lines and demultiplexes the cells occurring at the STS-48 rate and appearing on single incoming lines, on a 1-to-16 basis, into separate bit-serial lines feeding the input modules (a plurality of data demultiplexers, each data demultiplexer having a data input port at which a data stream S (single incoming line) is received, and each demulitplexer having a plurality of data output ports, as seen from 230 of figure 2 and col13 lines48-55).

a control switch module coupled to the switch fabric containing input modules and coupled to the demultiplexers (figure 2) which controls each of the blocks that constitute the switch, for example, processes incoming calls by establishing and tearing down appropriate virtual connections through the switch (global scheduler operatively coupled to said data demultiplexers and to each of said data input data queues, controlling the routing of data from said plurality of switch input ports to said plurality of switch output ports, col12 lines56-68).

of a demultiplexer that would precede input ports and convert an incoming STS-12 serial bit stream into four different STS-3c streams. Each of these streams feeds into four different corresponding input ports. That the STS-12 ATM cells, which are provided to the input ports of the associated input module, are sequentially entered in a

regular order into a single internal queue within that module, are also read from a single corresponding logical queue in a common output module in the same order, which will advantageously preserve the ordering of the bits on the STS-12 trunk entirely through the switch (dividing the delivery of data packet of data flows of an input data stream that is input to said data switch, and by computing a data packet schedule for each cross bar switch such that the temporal order of data packets into said data switch is maintained through each of the cross bar switches, col50 lines 50-66).

Cisneros however fails to specifically disclose each demultiplexer having a plurality of data output ports each of which is coupled to a separate one of the input data queues associated with each corresponding cross bar switch input port. Cisneros however discloses of deficiencies of switches can be ameliorated through various queuing functions and centralized control (col4 lines 34-39), thus providing the motivation to improve speeds of a switching system in a efficient and reliable manner.

Iyer further discloses the desire to build a very high speed packet-switch with extremely high line-rates, by building a packet-switch from multiple, lower speed packet-switches in parallel (abstract). From figure 1, discloses of a parallel packet switch architecture that when a cell arrives at an input port, the demulitplexer selects a layer (cross point plane) to send the cell to and that each of the layers receive cells from the N input ports, then switches each cell to its output port (page 3). It should be seen from figure 1 and figure 2, of an architecture that discloses each demultiplexer having a

plurality of data output ports each of which is coupled to a separate one of the input data queues associated with each corresponding cross bar switch input port. It would thus be obvious to a person skilled in the art to incorporate the architecture of a switching system as disclosed by Iyer into the apparatus and method for a large packet switch which utilizes cell address look-ahead in conjunction with parallel cross point planes as disclosed by Cisneros to efficiently improve the speed of a packet system in a reliable manner, more specifically the coupling of demultiplexer output ports to different switching layers and the switching plane's associated queue.

Regarding claim 5, Cisneros discloses a switch fabric comprising:

self-routing cross-point switching planes composed of identical cross-point switching planes (col17 lines 35-40) with each plane having 256 separate input and 256 separate output connections (a plurality of K cross bar switches, each cross bar switch having N switch input ports I, and N switch output ports O, 550 of figure 5 and col17 lines 57-59).

input modules, containing a single queue, that successively reads the current incoming ATM cells appearing at each of its inputs and deposits the cell into the next available location in the queue (col20 lines 9-16), wherein for any input module, each successive incoming line in the group is connected to a corresponding successive input port of that module and in addition, each of the input modules is connected to the same corresponding numerical input port on all of cross-point switching plane (at least one of

N parallel input data buffers B, each input data buffer B having an input port I, each input buffer of said N buffers further having an output O coupled to a single one of said N switch input ports such that data packets in each of said N, parallel input data buffers can be selectively routed into said corresponding crossbar switch, 250 of figure 5 and col18 59-68).

output modules, containing a single queue, which feeds from the cross-point switching planes. Each of the numerical outputs on any one of the switching planes feeds a common numerical input on every output module (col19 lines 22-26). Each of the output modules routes incoming switched ATM cells to one of the separate output ports available on that module which is connected to a corresponding output line (an output buffer, each output buffer having an input coupled to a single one of said N switch output ports of the corresponding cross bar switch and each output buffer having an output port from which data is transmitted to an output destination link, 270 of figure and col19 lines 45-49).

demultiplexers which accepts incoming cells from user lines and demultiplexes the cells occurring at the STS-48 rate and appearing on single incoming lines, on a 1-to-16 basis, into separate bit-serial lines feeding the input modules containing input ports I and a single queue (N data demultiplexers comprising of a data input port at which a data stream S is received, and N data output ports, each data output port being coupled to the input I, each of said data demultiplexers selectively routing certain data packets in said stream S to at least one of the input data buffer, 230 of figure 2 and col13 lines48-55).

a control switch module coupled to the switch fabric containing input modules and coupled to the demultiplexers (figure 2) which controls each of the blocks that constitute the switch, for example, processes incoming calls by establishing and tearing down appropriate virtual connections through the switch (a scheduler coupled to said N data demultiplexers, cross bar switches, and said N data input data buffers, said scheduler controlling the selective delivery of data packets into certain input data buffers and from said input data buffers into a corresponding cross bar switch, 290 of figure 2 and col12 lines56-68).

Cisneros however fails to specifically disclose each demultiplexer having a N data output ports each of which is coupled to a separate one of the input data queues associated with each corresponding cross bar switch input port. Cisneros however discloses of deficiencies of switches can be ameliorated through various queuing functions and centralized control (col4 lines 34-39), thus providing the motivation to improve speeds of a switching system in a efficient and reliable manner.

Iyer further discloses the desire to build a very high speed packet-switch with extremely high line-rates, by building a packet-switch from multiple, lower speed packet-switches in parallel (abstract). From figure 1, discloses of a parallel packet switch architecture that when a cell arrives at an input port, the demulitplexer selects a layer (cross point plane) to send the cell to and that each of the layers receive cells from the N input ports, then switches each cell to its output port (page 3). It should be seen from

figure 1 and figure 2, of an architecture that discloses each demultiplexer having a plurality of data output ports each of which is coupled to a separate one of the input data queues associated with each corresponding cross bar switch input port. It would thus be obvious to a person skilled in the art to incorporate the architecture of a switching system as disclosed by Iyer into the apparatus and method for a large packet switch which utilizes cell address look-ahead in conjunction with parallel cross point planes as disclosed by Cisneros to efficiently improve the speed of a packet system in a reliable manner, more specifically the coupling of demultiplexer output ports to different switching layers and the switching plane's associated queue.

Regarding claim 6, Cisneros discloses a switch fabric comprising:

self-routing cross-point switching planes composed of identical cross-point switching planes (col17 lines 35-40) with each plane having 256 separate input and 256 separate output connections (K cross bar switches, each of said K switches having N switch inputs ports I and N switch outputs ports O, 550 of figure 5 and col17 lines 57-59).

input modules, containing a single queue, that successively reads the current incoming ATM cells appearing at each of its inputs and deposits the cell into the next available location in the queue (col20 lines 9-16), wherein for any input module, each successive incoming line in the group is connected to a corresponding successive input port of that module and in addition, each of the input modules is connected to the same

corresponding numerical input port on all of cross-point switching plane (250 of figure 5 and col18 59-68) and reads a cell from the head of its internal queue (N input data FIFO buffers, each input data FIFO buffer having an input to which stream of data can be sent, each input data FIFO further having an output Bo coupled to a single switch input port Ij of said N switch input ports, each of said input data FIFO buffers storing data packets to be routed through the cross bar switches from switch input port Ij to a switch output port Ok, 250 of figure 5 and col20 lines 26-30).

a demultiplexer, containing input and output ports, that would precede input ports and convert an incoming STS-12 serial bit stream into four different STS-3c streams. Each of these streams feeds into four different corresponding input ports. That the STS-12 ATM cells, which are provided to the input ports of the associated input module, are sequentially entered in a regular order into a single internal queue within that module, are also read from a single corresponding logical queue in a common output module in the same order, which will advantageously preserve the ordering of the bits on the STS-12 trunk entirely through the switch (N data demultiplexers, each data demultiplexer having a data input port at which a data stream S comprised of a plurality of data flows is received, and further having N data output ports, each of said data demultiplexer selectively routing data packets of predetermined flows to at least one input I of said input data FIFO buffer, 230 of figure 2 and col50 lines 50-66).

a control switch module coupled to the switch fabric containing input modules and coupled to the demultiplexers (figure 2) which controls each of the blocks that constitute the switch, for example, processes incoming calls by establishing and tearing

down appropriate virtual connections through the switch (a scheduler coupled to said N data demultiplexers, said cross bar switches and said N data input data FIFO buffers, said scheduler being capable of directing data packets of at least one data flow, 290 of figure 2 and col12 lines56-68).

Cisneros however fails to specifically disclose each demultiplexer having a N data output ports each of which is coupled to a corresponding separate ones of the input data FIFO buffers at each switch input port of each of said K cross bar switches. Cisneros however discloses of deficiencies of switches can be ameliorated through various queuing functions and centralized control (col4 lines 34-39), thus providing the motivation to improve speeds of a switching system in a efficient and reliable manner.

Iyer further discloses the desire to build a very high speed packet-switch with extremely high line-rates, by building a packet-switch from multiple, lower speed packet-switches in parallel (abstract). From figure 1, discloses of a parallel packet switch architecture that when a cell arrives at an input port, the demulitplexer selects a layer (cross point plane) to send the cell to and that each of the layers receive cells from the N input ports, then switches each cell to its output port (page 3). It should be seen from figure 1 and figure 2, of an architecture that discloses each demultiplexer having a plurality of data output ports each of which is coupled to a separate one of the input data queues associated with each corresponding cross bar switch input port. It would thus be obvious to a person skilled in the art to incorporate the architecture of a

switching system as disclosed by Iyer into the apparatus and method for a large packet switch which utilizes cell address look-ahead in conjunction with parallel cross point planes as disclosed by Cisneros to efficiently improve the speed of a packet system in a reliable manner, more specifically the coupling of demultiplexer output ports to different switching layers and the switching plane's associated queue.

Regarding claim 7, Cisneros discloses each input module in the inventive switch has a single internal queue illustratively implemented using shared memory (input data FIFO buffers are comprised of random access memory, col7 lines42-45).

Regarding claim 12, 13, and 14, Cisneros discloses a switching system comprising:

cross-point switching planes on a parallel, through time staggered basis (a plurality of parallel-coupled cross-bar switching systems, col8 lines 12-14). It is further seen from figure 5 and figure 2 that the switching system comprises a demuliplexer (230 of figure 2, a plurality of input queues (queues of input modules, 260 of figure 5), and a cross bar switch (cross-point plane, 550 of figure 5). Cisneros further discloses that a demultiplexer, containing input and output ports, that would precede input ports and convert an incoming STS-12 serial bit stream into four different STS-3c streams (generate a plurality of outputs from an input stream.

a control switch module coupled to the switch fabric which controls each of the blocks that constitute the switch, for example, processes incoming calls by establishing

and tearing down appropriate virtual connections through the switch (global scheduler, operatively coupled to and controlling the flow of data into each of said cross-bar switching systems, 290 of figure 2 and col12 lines56-68) and that those cells that win arbitration are simultaneously applied by their respective input modules through the cross-point switching planes and routed there through to the addressed output modules for each cell through the input and output ports of the plane (computing at least one match of cross bar switching inputs to cross bar switching outputs, figure 5 and col7 lines 61-64) and that during each staggered time interval, every input module simultaneously provides output port address and cell priority information for the ATM cell presently situated at the head of its internal queue and routes to a specific cross-point plane (during a data cell time slot interval, col8 lines 18-38).

Cisneros however fails to specifically disclose that the demultiplexer is operable to provide each of the plurality of outputs to a separate one of the plurality of input queues, each input queue being associated with a particular input to the cross bar switch. Cisneros however discloses of deficiencies of switches can be ameliorated through various queuing functions and centralized control (col4 lines 34-39), thus providing the motivation to improve speeds of a switching system in a efficient and reliable manner.

Iyer further discloses the desire to build a very high speed packet-switch with extremely high line-rates, by building a packet-switch from multiple, lower speed packet-

switches in parallel (abstract). From figure 1, discloses of a parallel packet switch architecture that when a cell arrives at an input port, the demulitplexer selects a layer (cross point plane) to send the cell to and that each of the layers receive cells from the N input ports, then switches each cell to its output port (page 3). It should be seen from figure 1 and figure 2, of an architecture that discloses each demultiplexer having a plurality of data output ports each of which is coupled to a separate one of the input data queues associated with each corresponding cross bar switch input port. It would thus be obvious to a person skilled in the art to incorporate the architecture of a switching system as disclosed by Iyer into the apparatus and method for a large packet switch which utilizes cell address look-ahead in conjunction with parallel cross point planes as disclosed by Cisneros to efficiently improve the speed of a packet system in a reliable manner, more specifically the coupling of demultiplexer output ports to different switching layers and the switching plane's associated queue.

Allowable Subject Matter

5. Claims 8-11 are allowed.

The following is a statement of reasons for the indication of allowable subject matter:

6. Claim 8 is are allowable over the prior art of record since the cited references taken individually or in combination fails to particularly disclose **routing at least some of the data packets of the flow f1 to a data buffer B having the smallest amount of data waiting to be routed through its associated cross bar switch.** It is noted that the closest prior art, Cisneros et al. (US 5157654) discloses the technique and

apparatus for resolving output port contention in a high-speed packet switch. However, Cisneros fails to disclose or render obvious to the above underline limitations as claimed.

Conclusion

7. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nguyen Ngo whose telephone number is (571) 272-8398. The examiner can normally be reached on Monday-Friday 7am - 3:30 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ricky Ngo can be reached on (571) 272-3139. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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SUPERVISORY PATENT EXAMINER